PATENT AND TRADEMARK OFFICE

Patent Application

Inventors: Young-Kai Chen et al

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Examiner: Matthew C. Landau

Title: FLAT PROFILE STRUCTURES FOR BIPOLAR TRANSISTORS

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Sir:

This Appeal Brief is being filed under 37 C.F.R. § 41.37 within one month of the Oct. 12, 2007 mailing date of the Panel Decision on the Pre-Appeal Brief Review.

The Commissioner is authorized to charge the **$500** fee for the Appeal Brief under 37 C.F.R. § 41.20(b)(2) to **Deposit Account No. 12-2325**. In the event of a non-payment or an improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325,** as required to correct the error.

Respectfully,

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Date: Nov. 12, 2007
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ITEMS OF APPEAL BRIEF UNDER 37 C.F.R. § 41.37

i) Real party-in-interest

The real party-in-interest is Lucent Technologies Inc., 600-700 Mountain Ave., Murray Hill, NJ 07974-0636. Lucent Technologies Inc. is owner of the entire interest in the application-at-issue by an assignment recorded at Reel/Frame Nos. 014326/0796 on July 21, 2003.

ii) Related appeals and interferences

Appellants do not know of any prior and pending Appeals, Interferences, or Judicial Proceedings related to, directly affecting, directly affected by, or have a bearing on the Board's decision in this Appeal.

iii) Status of claims

Claims 8, 10, 12 – 14, 16 – 19, 22, 25, 29 – 31 are rejected.

Herein, the rejections of all of these claims are appealed.

In the Final Office Action, only pages 2 – 6 state claim rejections. Thus, any earlier claim rejections are either stated on those pages or are assumed waived. See 37 C.F.R. §§ 113(b), 104; M.P.E.P. § 706.07.

iv) Status of amendments

There were no amendments submitted after mailing of the Final Office Action.

v) Summary of claimed subject matter

Independent claim 1 features an integrated circuit (see e.g., Fig. 2 and page 3, lines 24 - 25). The integrated circuit includes a substrate (e.g., substrate 22 in Fig. 2 and at page 3, lines 28 - 31) having a top surface (e.g., surface 23 in Fig. 2 and at page 3, lines 28 - 31) and collector, base, and emitter semiconductor layers (e.g., layers 24, 25, 26 in Fig. 2 and at page 3, lines 28 - 32) of a bipolar transistor (e.g., transistor 20 in Fig. 2 and

at page 3, line 28). The semiconductor layers form a vertical sequence (e.g., sequence 24, 25, 26 in Fig. 2 and at page 3, lines 28 - 32) on the substrate in which intrinsic portions of two of the semiconductor layers (e.g., portion 28 and adjacent part of layer 26 in Fig. 2 and between page 3, line 32, and page 4, line 11) are sandwiched between the top surface of the substrate and a remaining top one of the semiconductor layers (e.g., layer 24 in Fig. 2). The base layer includes an extrinsic portion (e.g., portion 29 in Fig. 2 and between page 3, line 32, and page 4, line 1) that laterally encircles a vertical portion of the top one of the semiconductor layers (e.g., portion 29 and layer 24 in Fig. 2 and page 4, lines 1 - 2). The integrated circuit includes a dielectric sidewall (e.g., spacer 30 in Fig. 2 and at page 4, lines 12 - 13) being interposed between the vertical portion of the top one of the semiconductor layers and the extrinsic portion of the base layer (e.g., layer 24 and portion 29 in Fig. 2 and page 4, lines 12 - 13). The substrate includes a subcollector that forms an electrical contact for the collector layer (layer 27 in Fig. 2 and at page 3, lines 31 – 32, and page 4, lines 2 - 4). The entire subcollector is located outside of the portion of the substrate that is vertically below part of the base layer (see e.g., subcollector layer 27 and right extrinsic portion 29 of base layer 26 in Fig. 2).

vi) Grounds of rejection to be reviewed on appeal

A) Whether claims 8, 10, 12 – 14, 22, and 25 are novel under 35 U.S.C. § 102(b) over U.S. Patent 5,506,427 of Imai et al (Herein, referred to as Imai.).

B) Whether claim 17 is non-obvious under 35 U.S.C. § 103(a) over a combination of Imai as applied to claim 8 and U.S. Patent 5,444,003 of Wang et al (Herein, referred to as Wang.).

C) Whether claims 18 – 19 and 29 – 30 are non-obvious under 35 U.S.C. § 103(a) over a combination of Imai as applied to claim 8 and U.S. Patent 6,541,346 of Malik (Herein, referred to as Malik.).

D) Whether claim 31 is obvious under 35 U.S.C. § 103 over a combination of Imai and Malik as applied to claims 18 – 19 and 29 – 30 and U.S. Patent 5,096,844 of Konig et al (Herein, referred to as Konig.).

vii) Argument

A) Claims 8, 10, 12 – 14, 22, and 25 are novel over Imai, as applied at page 2 – 3 in the Final Office Action.

Claim 8

The Final Office Action relies on N^+-type layer 18 of Imai's Fig. 1H in the anticipation rejection of pending claim 8. To better explain the error in this rejection, Applicants reproduce below Imai's Figure 1H.

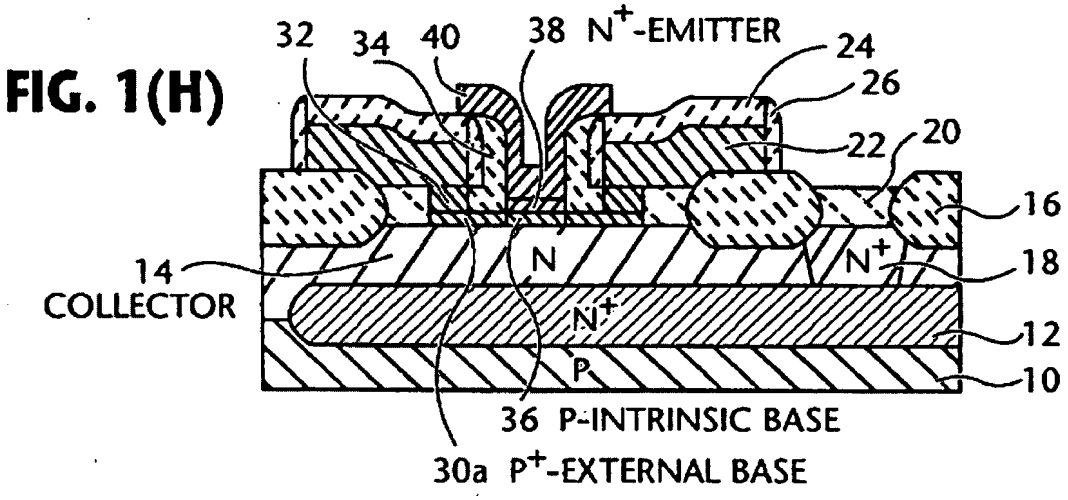

Figure 1H clearly shows N^+-type layer 18 as being located to the side of the layer 14 and clearly identifies layer 14 as the collector. That is, the parts of Imai relied on by the Final Office Action do not show the N^+-type layer 18 as being below the collector 14.

At page 3 line 1, and page 6, lines 11 – 13, the Office Action states that Imai's N^+-type layer 18 teaches a subcollector as recited in the pending claim 8. In response, Applicants must note that the term "subcollector" is descriptive. In particular, subcollector includes the prefix "sub" and the noun "collector". Since the prefix "sub" means "below", it is evident that the term subcollector must refer to a feature or layer that is located below the collector. Thus, Imai's N^+-type layer 18 cannot be a subcollector, because the N^+-type layer 18 is simply not located below Imai's collector 14. That is, while the Office Action indicates that Imai's N^+-type layer 18 is a subcollector, such an interpretation is inconsistent with the ordinary meaning of the term "subcollector". In particular, the Office Action has completely ignored the prefix "sub" of subcollector in identifying Imai's N^+-type layer 18 with a subcollector. For this reason, the Office

Action does not cite a proper prior art teaching for subcollector as recited in pending claim 8. Thus, the Office Action does not provide a proper case of anticipation, and the novelty rejection of claim 8 should be withdrawn.

For completeness, Applicants also mention that Imai's Fig. 1H does show another N^+-type layer 12 that may be identified as a "subcollector". The N^+-type layer 12 is buried below Imai's collector 14. Thus, the N^+-type layer 12 is located where a subcollector must be located. Nevertheless, the N^+-type buried layer 12 of Imai does not meet the limitations recited by pending claim 8 for the subcollector. In particular, pending claim 8 recites:

> wherein the substrate includes a subcollector that forms an electrical contact for the collector layer, the entire subcollector being located outside of the portion of the substrate that is vertically below part of the base layer.

(underlining added).

In contrast, Imai's Fig. 1H shows the N^+-type layer 12 as, at least, extending below each part of the base layer, e.g., it extends below elements 36, 30a, 32 and 22. Since Imai's N^+-type layer 12, at least, extends below the whole shown base layer, Imai does NOT teach that the entire N^+-type layer 12 is located outside of the portion of the substrate that is vertically below part of the base layer as recited in pending claim 8. Thus, even if the Examiner had correctly identified Imai's N^+-type layer 12 as a subcollector, the cited parts of Imai would not disclose that the N^+-type layer 12 satisfy the properties of the subcollector as recited in pending claim 8. For that reason, pending claim 8 should still be found to be novel over Imai if it is found that Imai's N^+-type layer 12 is a subcollector.

For the above-stated reasons, the novelty rejection of claim 8 should be withdrawn.

Claims 10, 12 – 14, 16, 22, and 25

Claims 10, 12 – 14, 16, 22, and 25 are novel over Imai as applied in the Office Action, at least, by their dependence on novel base claim 8. For this reason, the novelty rejections of claims 10, 12 – 14, 16, 22, and 25 should be withdrawn.

B) Claim 17 is non-obvious over Imai as applied to claim 8 when combined with Wang as in the Final Office Action.

Claim 17 is non-obvious over the above combination, at least, by its dependence on base claim 8, because the Final Office Action does not apply Wang to teach features of base claim 8. In particular, the Office Action has not provided a proper prior art teaching of a subcollector with the properties recited in base claim 8 and thus, has not provided a prima facie case of obviousness for dependent claim 17.

C) Claims 18 – 19 and 29 – 30 are non-obvious over Imai as applied to claim 8 when combined with Malik as in the Final Office Action.

Claims 18 – 19 and 29 – 30 are non-obvious over the above combination, at least, by their dependence on pending claim 8, because the Office Action does not apply Malik to teach elements of base claim 8. In particular, the Office Action has not provided a proper prior art teaching of a subcollector with the properties recited in base claim 8 and, thus, has not provided a prima facie case of obviousness for any of dependent claims 18, 19, 29, and 30.

D) Claim 31 is non-obvious over Imai and Malik as applied to claims 18 – 19 and 29 – 30 when combined with Konig as in the Final Office Action.

Claim 31 is non-obvious over the above combination, at least, by its dependence on pending claim 8, because the Office Action does not apply Malik or Konig to teach elements of base claim 8. Thus, the Office Action has not provided a proper prior art teaching of a subcollector with the properties recited in base claim 8 and thus, has not provided a prima facie case of obviousness for dependent claim 31.

viii) Claims appendix

1 – 7. (canceled)

8. (previously presented) An integrated circuit, comprising:

a substrate having a top surface;

collector, base, and emitter semiconductor layers of a bipolar transistor, the semiconductor layers forming a vertical sequence on the substrate in which intrinsic portions of two of the semiconductor layers are sandwiched between the top surface of the substrate and a remaining top one of the semiconductor layers, the base layer comprising an extrinsic portion that laterally encircles a vertical portion of the top one of the semiconductor layers; and

a dielectric sidewall being interposed between the vertical portion of the top one of the semiconductor layers and the extrinsic portion of the base layer; and

wherein the substrate includes a subcollector that forms an electrical contact for the collector layer, the entire subcollector being located outside of the portion of the substrate that is vertically below part of the base layer.

9. (canceled)

10. (previously presented) The integrated circuit of claim 8, wherein the extrinsic portion of the base layer extends farther away from the substrate than an interface between the top one of the semiconductor layers and the base layer.

11. (canceled)

12. (previously presented) The integrated circuit of claim 8, wherein a part of the extrinsic portion of the base layer is located between the substrate and an extrinsic portion of the top one of the semiconductor layers.

13. (previously presented) The integrated circuit of claim 12, further comprising a

dielectric layer, a portion of the dielectric layer being located on the extrinsic portion of the base layer and the extrinsic portion of the top one of the semiconductor layers being located on the dielectric layer.

14. (previously presented) The integrated circuit of claim 12, wherein the extrinsic portion of the base layer extends farther away from the substrate than an interface between the top one of the semiconductor layers and the base layer.

15. (canceled)

16. (previously presented) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers is epitaxially grown.

17. (previously presented) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers is a graded layer.

18. (previously presented) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers includes gallium.

19. (previously presented) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers includes an InP layer.

20 – 21. (canceled)

22. (previously presented) The integrated circuit of claim 12, wherein the dielectric sidewall has a thickness of 500 to 1500 angstroms.

23 – 24. (canceled)

25. (previously presented) The integrated circuit of claim 14, further comprising a dielectric layer, a portion of the dielectric layer being located on the part of the extrinsic

portion of the base layer and the extrinsic portion of the top one of the semiconductor layers being located on the dielectric layer.

26 – 28. (canceled)

29. (previously presented) The integrated circuit of claim 8, wherein the base layer comprises gallium.

30. (previously presented) The integrated circuit of claim 8, wherein the base layer comprises gallium, indium and arsenic.

31. (previously presented) The integrated circuit of claim 8, wherein the substrate is an InP substrate.

ix) Evidence appendix

None.

x) Related proceedings appendix

None.